Amendments to the Claims:

This listing of claims will replace all prior versions of the claims in the present application:

Listing of Claims:

1. (Currently Amended) A method for automatically determining a configuration of an I/O connector panel coupled to a system, the method comprising:

providing information about the capabilities of the I/O connector panel to a memory within the I/O connector panel, prior to connecting one or more peripherals to the I/O connector panel;

examining the information in the memory; and

downloading at least one driver to the [[a]] system coupled to the I/O connector panel based upon the examined information.

2. (Canceled)

3. (Original) The method of claim 1 wherein the downloading step is provided by software that is independent of the type of I/O connector panel.

4. (Currently Amended) The method of claim 1 wherein the system includes a core PC function block that is configured independently of the I/O connector panel.

5. (Currently Amended) An I/O connector panel comprising:

a plurality of I/O connectors; and

a memory containing information about the capabilities of the I/O connector panel, prior to connecting one or more peripherals,

wherein, when the memory is examined, at least one driver can be downloaded to a system coupled to the I/O connector panel.

6. (Currently Amended) The I/O connector panel of claim 5 wherein the memory comprises an EEPROM.

7. (Currently Amended) The I/O connector panel of claim 5 wherein the system includes a core PC function block.

8. (Currently Amended) The I/O connector panel of claim 5 further comprises connector logic coupled to the memory for I/O distribution.

9. (Currently Amended) The I/O connector panel of claim 5 wherein the memory contains attributes of the I/O connector panel and attributes of each connector installed on the connector panel.

10. (Currently Amended) A processing system comprising:

a core PC function; and

at least one I/O connector panel coupled to the core PC function, the at least one I/O connector panel comprising:

a plurality of I/O connectors; and

a memory containing information about the capabilities of the I/O connector panel prior to connecting one or more peripherals, wherein, when the memory is examined, at least one driver can be downloaded to the core PC function ~~a system~~ coupled to the I/O connector panel.

11. (Original) The processing system of claim 10 wherein the memory comprises an EEROM.

12. (Original) The processing system of claim 10 further comprises connector logic coupled to the memory for I/O distribution.

13. (Original) The processing system of claim 10 wherein the memory contains attributes of the I/O connector panel and attributes of each connector installed on the I/O connector panel.

14. (Currently Amended) A processing system comprising:

a core PC function; and

a plurality of I/O connector panels coupled to the core PC function, each of the plurality of I/O connector panels comprising:

a plurality of a I/O connectors, an EEROM containing information about the capabilities of the I/O connector panel prior to connecting one or more peripherals, wherein, when the memory is examined, at least one driver can be downloaded to the core PC function ~~a system~~ coupled to the I/O connector panel; and

connector logic coupled to the EEROM for I/O distribution.

15. (Original) The processing system of claim 14 wherein the memory contains attributes of the I/O connector panel and attributes of each connector installed on the I/O connector panel.

16. (New) The method of claim 1, further comprising the steps of:

connecting the one or more peripherals to the I/O connector panel.